Scope: This document specifies the API for the command and control library for the MRS900 EchoLogger sonar.

Notes on Jetson:

CHAPTER 36: UART CONTROLLER

There are four Universal Asynchronous Receiver/Transmitters (UARTs) built into Tegra® X1 devices. These UARTs support

both 16450 and 16550 compatible modes. A fifth UART is located in the Audio Processing Engine (APE).

36.1 Functional Description

36.1.1 UARTs A through D

All UARTs provide serial data synchronization and data conversion (parallel-to-serial and serial-to-parallel) for both receiver and

transmitter sections. Synchronization for serial data stream is accomplished by adding start and stop bits to the transmit data to

form a data character. Data integrity is accomplished by attaching a parity bit to the data character. The parity bit can be

checked by the receiver for any transmission bit errors.

The interface supports word lengths from five to eight bits, an optional parity bit, and one or two stop bits. If enabled, parity can

be odd, even, or forced to a defined state. Interrupts can be generated from any of 10 sources.

The UART controller supports both 16450 and 16550 compatible modes. The default mode is 16450. This mode provides

independent 16-byte FIFOs for transmit and receive operations and is selected by the FIFO control register. It also includes a

16-bit programmable baud rate generator and an 8-bit scratch register, 8 modem control lines, and 2 DMA handshake lines that

are used to indicate when the FIFOs are ready to transfer data to the CPU.

The UARTs support a device clock of up to 200 MHz. Each symbol requires 16 clock cycles for proper sampling and processing

of the input data stream. Thus, the maximum baud rate is 200/16 = 12.5M. Because 1 symbol = 1 bit, the data rate is 12.5 Mbps.

All four UARTs are identical.